REMARKS:

Claims 26-33 and 40 have been allowed. The Office Action indicates that claims 7-10, 15-22, 35-37, 43, and 44 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicants contend for the following reason that the independent claims from which claims 7-10, 15-22, 35-37, 43, and 44 depend (directly or indirectly) are patentable, and thus that claims 7-10, 15-22, 35-37, 43, and 44 are patentable.

Claims 1-6, 11-14, 22-25, and 38-42 stand rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,945,855 ("Momtaz") in view of US Patent App. Pub. No. 2002/0027457 ("Chang"). In response, Applicants respectfully contend that these claims are patentable over the cited references for the following reasons.

Neither Momtaz nor Chang teaches or suggests a clock and data recovery device for generating data samples in response to data having jitter that:

includes phase detection circuitry configured to generate feedback indicative of the amount of the jitter and of phase error between a data sampling clock and the data, as recited in claim 1 or 38, or

includes clock control circuitry, coupled and configured to generate feedback indicative of the amount of the jitter and of phase error between a data sampling clock and the data, as recited in claim 12 or 39, or

includes a data loop configured to operate in response to an edge sampling clock and data samples generated by sampling circuitry to generate feedback indicative of the amount of the jitter and of phase error between a data sampling clock and the data, as recited in claim 40.

Nor does either Momtaz or Chang teach or suggest a method for sampling data having jitter, including a step of generating a charge pump current in response to feedback, where the feedback is indicative of phase error between a data sampling clock and the data, and the feedback is also indicative of the amount of the jitter, as recited in claim 41.

An example of feedback indicative of the amount of jitter of data being sampled, as recited, is the output of jitter estimating circuitry 90, 92, and 93 of Fig. 12(a) of the present application. The following are examples of the feedback generated by this circuitry which is

indicative of the amount of jitter of data (being sampled by a clock and data recovery device): a "strong down" code word that indicates a small amount of jitter in the data, a "weak down" code word that indicates a greater amount of jitter, a "stay" code word that indicates a greater amount of jitter, a "weak up" code word that indicates a greater amount of jitter, and a "strong up" code word that indicates a still greater amount of jitter.

To the extent pertinent, Momtaz's teaching (e.g., at col. 3, lines 6-10, 48-53, and 64-67, with reference to Fig. 1) is merely that a data recovery device for generating data samples should include circuitry (e.g., phase detector 11) that generates feedback of indicative of phase error between the data being sampled and a data sampling clock. There is no teaching or suggestion determinable from Momtaz that the feedback is or should be indicative of the amount of jitter of the data. Specifically, Momtaz teaches that phase detector 11 should determine phase error between the data and a data sampling clock and should generate and assert charge pump control signals 16 and 18 in response to this determination. The control signal 16 ("UP") is asserted when the phase of the data leads the phase of a VCO clock. The control signal 18 ("DN") is asserted when the phase of the data lags the phase of the VCO clock. Momtaz's "UP" and "DN" signals apparently correspond to the "up_i" and "$down_i$" bits that are input to the jitter estimating circuitry 90, 92, and 93 of Fig. 12(a) of the present application; not to feedback of the type recited (e.g., feedback generated by jitter estimating circuitry 90, 92, and 93). Momtaz's "UP" and "DN" signals apparently are not themselves indicative of the amount of jitter in data being sampled.

Further, there is no teaching or suggestion determinable from Momtaz or Chang of clock control circuitry (as recited in claim 1 or 38) that is coupled and configured to generate a control signal in response to feedback (of the type recited in claim 1 or 38), wherein the control signal is at least substantially independent of the amount of jitter (in data being sampled) over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval; or

clock control circuitry, coupled and configured to generate charge pump current (as recited in claim 12 or 39) in response to feedback (of the type recited in claim 12 or 39), wherein the charge pump current has an average current value, I_{avg}, that is at least substantially independent of the amount of jitter (in data being sampled) over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the

phase error between the data sampling clock and the data over the time interval, and I_{avg} is an average of instantaneous values of the charge pump current over said time interval; or

a data loop including clock generation circuitry (as recited in claim 40) configured to generate a control signal in response to feedback (of the type recited in claim 40) such that the control signal is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval.

The Office Action identifies no such teaching or suggestion determinable from Momtaz or any other reference of record. Momtaz fails to provide such teaching or suggestion at col. 3, lines 59-63, or elsewhere.

Further, there is no teaching or suggestion determinable from Momtaz or Change of a method for sampling data having jitter, including a step of generating a charge pump current (as recited in claim 41) in response to feedback (of the type recited in claim 41), the charge pump current having an average current value that is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of said phase error over the time interval, and the average current value is an average of instantaneous values of the charge pump current over said time interval. The Office Action identifies no such teaching or suggestion determinable from Momtaz or any other reference of record.

Claims 34 and 35 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,604,775 ("Saitoh"). In response, Applicants respectfully contend that these claims are patentable over Saitoh for the following reasons.

Claim 34 recites a jitter estimating circuit for use in an clock and data recovery device configured to generate samples of data having jitter using a data sampling clock, where the clock and data recovery device is configured to generate the data sampling clock by applying variable delay to a first clock, said circuit including counter circuitry configured to generate a sequence of counts in response to feedback indicative of phase error between the data sampling clock and the data, wherein each of the counts is indicative of the number of times that the clock and data recovery device changes the phase of the first clock during a predetermined number of valid transitions of the data.

Saitoh fails to teach or suggest a jitter estimating circuit including counter circuitry of the type recited in claim 34. The Office Action asserts that "up-down counter" 42 of Saitoh's Fig. 3 is an example of the recited counter circuitry. However, Saitoh's counter 42 apparently merely counts the number of cycles of a reference clock (the reference clock asserted to both counter 42 and variable delay line 10), with counter 42 counting up whenever control signal "U/D" is equal to "0" and counter 42 counting down whenever signal "U/D" is equal to "1" (as described at Saitoh's col. 8, lines 35-52). Control signal U/D is generated as described with reference to Saitoh's Figs. 8 and 9, and has a rising edge when the output "PD" of phase detector 30 indicates that the reference clock's phase leads that of a delayed version of the reference clock. There is apparently no teaching or suggestion determinable from Saitoh that the output of counter 42 (or any other counter of Saitoh's apparatus) is indicative of the number of times that a clock and data recovery device changes the phase of a first clock during a predetermined number of valid transitions of the data.

Thus, each of claim 34 and claim 35 (which depends from claim 34) is patentable over Saitoh.

Respectfully submitted,

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